RF Analysis of a Sub-GHz InP-Based 1550 nm Monolithic Mode-Locked Laser Chip

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***Abstract*— We report a monolithic sub-GHz repetition rate mode-locked laser with record low pulse-to-pulse RMS timing jitter of 3.65 ps in the passive mode locking regime. We analyse the optical pulse generation in passive and hybrid mode-locking operating regimes, finding narrower RF tone linewidth in the passive regime, attributed to the improved contact structure of the gain sections. The noise performance is also characterized in passive and hybrid regimes, showing RMS integrated timing jitter of approximately 600 fs. For hybrid modelocking, the repetition rate can be varied over a large range from 880 to 990 MHz. We observe broad pulse widths of few hundred picoseconds attributed to the (long folded) waveguide architecture and on-chip multimode interference mirrors. This device subjects a stand-alone, ultra-compact, mode-locking based clock source to realize frequency synthesizers operating over a frequency range from sub-GHz up to approximately 15 GHz.**

***Index Terms*— Mode-locked laser chip, timing jitter, amplitude noise, RF response.**

I. Introduction

MODE locked laser diodes (MLLDs) are promising candidates for signal sources in photonic radar systems, wireless data transmission, and frequency comb spectroscopy. Photonic integrated MLLD have been developed, reporting repetition rates starting in the microwave range (3 GHz to 30 GHz). The small size of the chips, combined with coupled-cavity effects, allowed reaching up into the Terahertz range (300 GHz to 3 THz). The generated electrical signal quality depends on the key parameters of the optical pulse train such as the pulse-to-pulse duration, the width of the generated optical spectrum and the optical linewidth, which strongly depend on the type of mode-locking and laser architecture [1]. One of the key challenges for MLLD is to achieve low repetition rates (from 100 MHz to 3 GHz), of interest for applications such as dual comb spectroscopy, which require very long cavities. Recently, different MLLD structures have demonstrated repetition rates below 10-GHz, fabricated on monolithic indium phosphide (InP) active-passive integration platform as well as on heterogeneous silicon/III–V platform.

With the heterogenerous approach, integrating a III-V gain section and saturable absorber on a passive silicon-on-insulator which included a 37,4 mm passive cavity terminated in a high-reflective Bragg mirror, 1 GHz repetition rate was reached. The measured autocorrelation trace FWHM and the linewidth of the fundamental beat note were 11ps and 2kHz respectively, assumed to be associated to the long passive cavity [2]. The key advantage of the monolithic approach is that it allows to fabricate all the required elements on a single chip, providing the most compact solution. Monolithic Indium Phosphide (InP) MLLD with low repetition rate have been recently reported. The lowest frequency achieved to date is 1-GHz [3], with a 41 mm linear resonator cavity using folded spiral passive optical waveguides and multimode interference reflector mirrors. In this laser, the electrical linewidth of the passive mode locking regime was 398 kHz, and the measured pulse duration reached 272 ps. A monolithic 2,5-GHz MLLD with 33-mm ring cavity structure was also reported, which in the passive mode-locking regime showed a low fundamental beat note linewidth of 6 kHz and 10 ps pulse duration [4].

In this paper we present a 1-GHz structure, similar to the one reported in [3], in which the semiconductor optical amplifier (SOA) sections are short-circuited in the chip having the same contact pad, which avoids injection current asymmetries. The long-cavity MLLD structure has been optimized to reduce the device footprint by folding of the elements appropriately. The comparison of the reported MLLD structures operating below 5 GHz is shown in Table I, including the structure in this work.

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We investigate the stability of the optical pulse behavior in both passive and hybrid mode-locking (HML) operation, optimizing the RF access to the chip. For the hybrid operating regime, we report the design of an optimized RF access through characterization of the RF signal paths. Our analysis shows the potential of implementing this chip as a stand-alone, extremely-compact clock source in microwave frequency synthesizers [3]. We showed that this optimized structure achieves a record low pulse-to-pulse RMS timing jitter of 3.65ps.

TABLE I
OVERVIEW OF MONOLITHIC MODELOCKED LASER DIODES OPERATING BELOW 5 GHZ REPETITION RATE

Parameter	unit	Ref. [2]	Ref. [3]	Ref. [2]	This work
Material[1]		Hetero	Mono	Mono	Mono
Cavity Length	mm	37.4	40.5	33	40.5
Repetition Rate	GHz	1	1	2.5	0.946
Structure		Linear	Linear	Ring	Linear
PML[2] – Linewidth	kHz	2	398	6.13	70
PML[2] – Pulsewidth	ps	5.5	-	9.8	500
HML[2] – Linewidth	kHz	-	< 1 Hz[3]	< 1 Hz[3]	< 1 Hz[3]
HML[2] – Pulsewidth	ps	-	272	-	200

[1] Hetero = Heterogeneous, Mono=Monolithic
[2] PML = Passive mode-locking, HML = Hybrid mode-locking
[3] Determined by RF source linewidth, limited by 1Hz resolution bandwidth

II. EXPERIMENTAL SETUP

The laser chip is fabricated over a 40.5mm waveguide length, embedded in an active-passive form. While the driving forward current is applied over an active length of 1.5mm, the rest is left as a passive waveguide and formed in two large spools where an ultra-compact geometry of 4.5mm × 1mm is achieved. Each passive-waveguide spool is terminated by a multimode interference reflector (MIR) [4]. This MIR is etched deeply to reflect part of the light back by total internal reflection principle, couple out the rest as an optical output. Hence, the laser resonator is realized between the two MIRs. A 50µm isolated segment is realized in the middle of the active gain section, and can be driven separately with a reverse bias to act as a saturable absorber. The laser output is achieved by the signal coupled out from MIR1. In contrast, the signal coupled out from MIR2 is amplified by pumping an embedded booster electrically via a forward current, and guided subsequently towards an on-chip photodiode (PD). The chip is attached to a custom-designed printed circuit board (PCB). The PCB is mounted on an aluminum holder where its temperature is set to 17 °C through a Peltier element.

Fig. 1 shows an illustrative image of the electronic schematic of the designed PCB along with an illustration of the laser chip. The designed schematic allows operating the laser chip in both passive and hybrid mode-locking schemes. The passive mode-locking (PML) scheme is realized by applying a forward current to the gain section and a reverse voltage into the absorber segment. In contrast, to realize the HML, the absorber segment is RF modulated. The modulating RF signal is generated from an electronic synthesizer and combined with the applied reversed DC voltage by utilizing a surface mounted bias tee. Another bias tee is introduced to enable applying an independent reversed bias voltage into the PD and realize an RF output signal which can be investigated with an electrical spectrum analyzer (ESA).

For characterization, the emitted light is collimated behind the chip utilizing an aspheric lens, where it is subsequently coupled into a standard single-mode fiber (SMF-28) to avoid

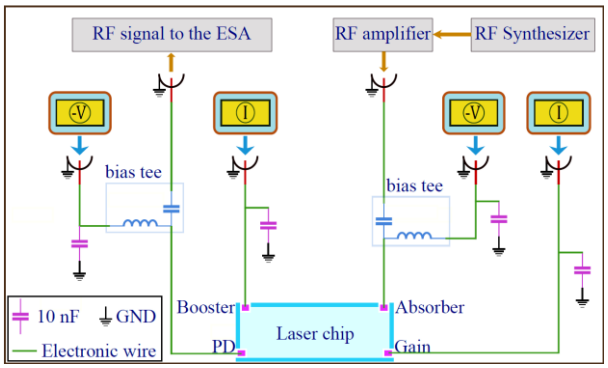

Fig. 1. Schematic design of the electronic driving circuit.

any perturbation of the mode-locking operation. The SMF-28 is physically coupled to an optical isolator. The optical signal is amplified afterwards utilizing a semiconductor optical amplifier (SOA), Thorlabs BOA1004P. The signal is subsequently optically divided by a sequence of fiber beam splitters (FBS), and investigated using an optical spectrum analyzer (OSA, Yokogawa), ESA (Rohde & Schwarz FSV7), and an oscilloscope (Lecroy SDA 830Zi-B) which features 30GHz bandwidth and provides sampling up to 80GS/s.

III. PASSIVE MODE-LOCKING

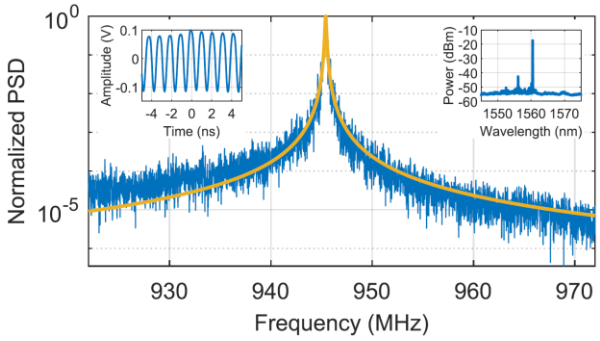

Fig. 2. Measured linewidth of the laser chip in PML operation. The Lorentzian fit features a linewidth of 70.75kHz and a corresponding pulse-to pulse jitter of 3.65ps. Left inset: Corresponding pulse-sequence. Right inset: Corresponding optical spectrum.

To realize the PML operation, we varied the gain current (GC) from 0mA to 200mA in steps of 1mA and the reverse voltage from 0V to −6V in steps of −0.1V. The best PML noise performance is achieved when the laser is driven at 143mA GC and the absorber is biased to −3.7V. At these parameters, the laser is operating at 946MHz, and the power spectral density

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(PSD) of the fundamental harmonic can be noticed in Fig. 2. In PML, the PSD features typically a Lorentzian-shape. Two parameters are typically defined to estimate the pulse-to-pulse RMS timing jitter: center frequency and the 3dB bandwidth of the Lorentzian PSD, Δf_{RF} [5]. Both parameters are extracted from the Lorentzian fit by scanning a short span and narrow resolution bandwidth (RBW). Δf_{RF} of 70.75kHz is extracted at 946MHz center frequency. The measured pulse-to-pulse RMS timing jitter amounts to 3.65ps. This low value of timing jitter for a low RR laser, manifests the stable pulse-sequence with low noise [6]. For the integrated RMS timing jitter, it can be observed from Fig. 2 that the Lorentzian fit and the measured PSD are approximately matched up to 8MHz from the peak at each side. Therefore, for a frequency offset range from 1MHz up to 8MHz, chosen to include as much phase noise as possible, the integrated RMS timing jitter amounts to 23.63ps which is approximately 2% of the average round trip time (1.056ns) of the laser. It is worth mentioning that the booster is driven at 0mA, to avoid any parasitic signal which might perturb the mode-locking behavior. The pulse-sequence while PML operation, is depicted in left inset of Fig. 2. Its corresponding optical spectrum can be seen in right inset of Fig. 2. We attribute the spectral narrowing and the rather long pulses (~ 500 ps) to the MIR which exhibits a fundamental limitation, featured by strong spectral filtering. Next, the RF performance of the laser system is analyzed.

IV. RF Analysis

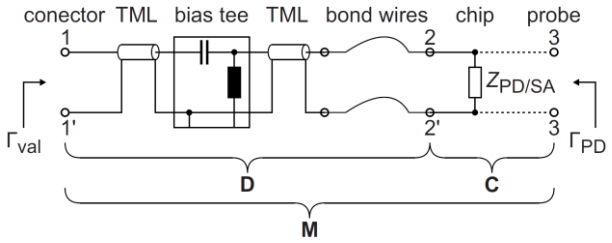

Fig. 3. Schematic of the RF signal path from the PCB connector (1) to the on-chip PD/SA (2) and the optional RF probe (3) with annotated measurable two-port network M, chip-probe network C, desired two-port network D.

Fig. 3 depicts a generic schematic of an RF signal path. Port 1 is the PCB connector, which is connected to an RF source or analyzer at the reference impedance Z0 = 50Ω. On the PCB the RF signal is transmitted via transmission lines (TML) and a bias tee to the bond wires. The TMLs are implemented as microstrip with Z0 [7]. The bond wires connect the TMLs to the laser chip, whose RF pad is port 2. The internal structures of the PD or SA are modelled by

$$Z_{PD/SA} = \left(R_{PD/SA} + j \cdot 2\pi C_{PD/SA}\right)^{-1} \quad (1)$$

with a shunt resistance RPD/SA and capacitance CPD/SA.

For the RF design the measures of interest are the desired two-port network D from port 1 to 2 and the RF power transmission from the 50Ω signal source or analyzer into the SA or PD and vice versa. However, measuring these is challenging. On the one hand, an additional optical transmitter or receiver can be used [8], [9]. However, this comprehends the undesired RF-to-optical conversion. Hence, optimizing just the RF power transmission is not feasible. On the other hand, only the reflected RF power and thus the reflection coefficient at port 1 can be measured [10]. However, the RF power absorbed by the network D and the PD cannot be distinguished. Thus, an optimization can result in increasing the RF power absorbed by the network D instead of the PD. To overcome these disadvantages, a method to de-embed D and calculate the RF power transmission is presented and exemplarily applied to the PD. Therefore, an RF probe (Picoprobe 67A) is used to directly contact the chip and offer an additional port 3.

The first RF measurement is conducted without bond wires and only attaching the RF probe to the chip. Therefore, the reflection coefficient Γ_{PD} is obtained by a Vector Network Analyzer (VNA) connected and calibrated to the RF probe. The resulting impedance of the PD is

$$Z_{PD} = Z_0 \cdot \frac{1+\Gamma_{PD}}{1-\Gamma_{PD}}, \quad \Gamma_{PD} = \frac{Z_{PD}-Z_0}{Z_{PD}+Z_0} \quad (2)$$

The second RF measurement is conducted with bond wires and attaching the RF probe to the chip. Then the two-port network M, from port 1 to 3, is directly measurable with the VNA connected and calibrated to the PCB connector and the RF probe. The third RF measurement is conducted in the operational setup, i.e. with bond wires and without RF probe, for validation. Thus, the reflection at port 1, Γ_{val}, is measured with the VNA.

The S-parameter matrix S, and ABCD-parameter matrix A are used to describe networks [11]. With Z_{PD} from the first RF measurement, the chip-probe network C from port 2 to 3 is

$$A_C = \begin{bmatrix} 1 & 0 \\ {Z_{PD}}^{-1} & 1 \end{bmatrix}, \; {A_C}^{-1} = \begin{bmatrix} 1 & 0 \\ -{Z_{PD}}^{-1} & 1 \end{bmatrix} (3)$$

With the A matrices, the relation of the two-port networks is

$$A_M = A_D \cdot A_C, \quad A_D = A_M \cdot A_C^{-1} \quad (4)$$

Utilizing (3), (4) and A_M from the second RF measurement, the desired network A_D and thus S_D can be calculated. As $Z_{PD} \neq Z_0$, the power transmission from port 1 to the PD is

$$G_{PD,1} = \frac{|S_{D,21}|^2}{1-|\Gamma_{in}|^2} \cdot \frac{1-|\Gamma_{PD}|^2}{|1-S_{D,22}\cdot\Gamma_{PD}|^2} (5)$$

$$\Gamma_{in} = S_{D,11} + \frac{S_{D,12}\cdot S_{D,21}}{\Gamma_{PD}^{-1} - S_{D,22}} \quad (6)$$

The resulting power transmission $G_{PD,1}$ in this case is around −11dB at f_{mod}= 880-MHz and −16dB at f_{mod} = 990-MHz.

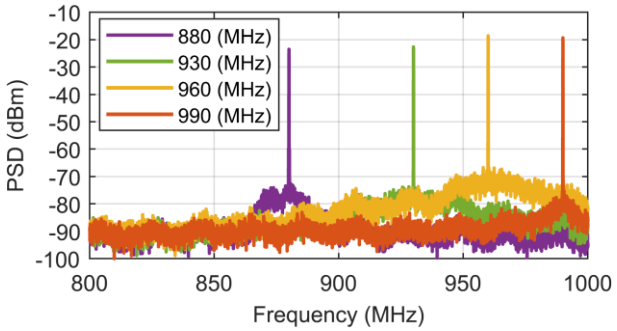

Fig. 4. RF spectra for a HML operation at f_{mod} of, 880MHz, 930MHz, 960MHz, and 990MHz.

This RF analysis enabled us to optimize the RF access to add an RF signal from a Continuous Wave source to the bias level

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on the Saturable Absorber to analyse the pulse sequence and timing jitter under hybrid mode locking (HML) regime.

V. Hybrid Mode-Locking

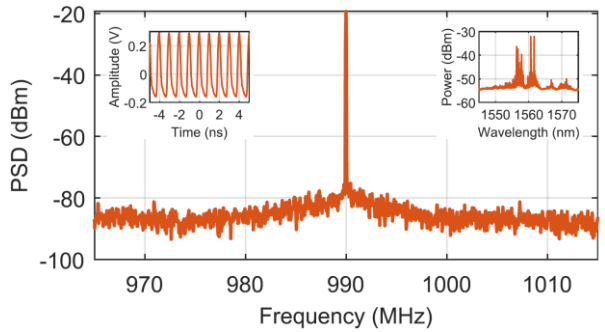

Fig. 5. RF spectrum at 990MHz f_{mod} . Left inset: pulse-sequence. Right inset: optical spectrum.

For HML, we modulated the absorber segment with a modulation frequency, f_{mod}, generated from an RF synthesizer (Analog Devices ADF4351) and amplified by an RF amplifier (Mini-Circuits ZFL-1000VH2B+) up to 25dBm. While the absorber voltage is biased identically to the PML operation, at −3.7V, the GC is varied to feature noise-burst-free HML performance. The f_{mod} is varied over a broad range, from 800MHz up to 1000MHz. Fig. 4 shows the fundamental RF spectra of the laser for nominal f_{mod} of 880MHz, 930MHz, 960MHz, and 990MHz. Though the HML is recognized over a broad RF spectral range, highest stability performance of the pulse-sequence is achieved at 880MHz and 990MHz f_{mod}. The HML phase noise performance approximately corresponds to that of the RF synthesizer at these modulation frequencies. Thus, RMS integrated timing jitter down to 550fs and 600fs, is measured at 880MHz and 990MHz f_{mod} for a phase noise integration range from 20kHz up to 100kHz offset frequency, respectively. Fig. 5 demonstrates the HML operation at nominal f_{mod} of 990MHz. The spectrum shows a typical HML performance where the f_{mod} features a needle shape on the top of a suppressed amplitude noise-band. The pulse-sequence and its corresponding optical spectrum are depicted in the left and right insets of Fig. 5, respectively. An optical pulse-width of 200ps and 335ps, is measured at 880MHz and 990MHz f_{mod}, respectively. In general, it can be observed that the optical spectrum is considerably narrow and exhibits spectral shift and variation in the pronounced modes depending on the applied f_{mod} in the HML regime. This can be attributed to the implemented MIRs which may stimulate modal dispersion that allows an internal mode distribution over the chip length. As a result, higher-order lateral modes may survive, and consequently enable a frequency distribution and strong spectral filtering. This probably also explains the observed broad locking modulation range of the laser chip.

VI. Conclusion

In conclusion, optical pulse generation from a sub-GHz InP on-chip monolithic mode-locked laser at 1550nm wavelength, is reported. In PML regime, a sequence of long optical pulses with low timing jitter at 946MHz repetition rate is generated. To further expand the investigation beyond PML operation, RF analysis of the laser system is conducted, since it is essential to accomplish the best HML performance. Thus, HML is achieved for repetition rates varying by more than 10%, i.e. from 880 to 990MHz. Hence, RMS integrated timing jitter down to 550fs (600fs) and an optical pulse-width of 200ps (335ps), are measured at 880MHz (990MHz) modulation frequencies, whilst operated in HML regime. This system introduces an ultra-compact mode-locked laser, operating in the sub-GHz range with high potential to be embedded as a clock-source in frequency synthesizers for the first time, according to our knowledge.

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